

REMARKS

The above-referenced patent application has been reviewed in light of the Office Action, mailed **May 1, 2006** (“the Action”) in which claims 1, 7 and 12 are rejected under 35 U.S.C. § 102(b) as being anticipated by Cho et al. (US Patent 6,021,506 – “Cho”). Also claims 1–16 are rejected under 35 U.S.C. § 102(b) as being anticipated by Yu et al. (US Patent 6,463,542 – “Yu”).

Current Status of Claims:

With this amendment, claims 1-16 remain pending. Claims 1, 7 and 12 are amended as presented above. No new matter has been introduced.

Independent claim rejections under 35 U.S.C. § 102(b) - Cho:

Claim 1, as currently amended, is as follows:

“A method comprising:

receiving an electrical idle ordered set at a receiving device power management unit, the electrical idle ordered set to indicate to the receiving device that a transmitting device coupled to the receiving device via an interconnect is to enter a low power state;

entering a low power entry state if there is no activity on the interconnect *based on receipt of the electrical idle ordered set;*
and

bypassing the low power entry state and entering a low power reset state if there is activity on the interconnect.”

Emphasis added.

Cho does not expressly or inherently describe the above emphasized elements of claim 1.

Cho describes powering down an AGP bus based on a *lack of graphics activities* over the AGP

bus. See Col 4, lines 20–37. Applicants submit that Cho’s focus is purely on graphics activities to determine whether to power down the AGP bus. Applicants submit that Cho does not include any description of receipt of an electrical idle ordered set as called for in claim 1 above. Thus, Applicants request withdrawal of the claim 1 rejection under 35 U.S.C. § 102(b) as being anticipated by Cho.

Independent claims 7 and 12 also include elements similar to those emphasized above for claim 1. Thus, Applicants also request withdrawal of the claim 7 and 12 rejections under 35 U.S.C. § 102(b) as being anticipated by Cho.

Claim rejections under 35 U.S.C. § 102(b) - Yu:

Relevant portions of claim 1, as currently amended, are as follows:

“A method comprising:
receiving an electrical idle ordered set..., the electrical idle ordered set to indicate to the receiving device that a transmitting device coupled to the receiving device via an interconnect is to enter a low power state;
entering a low power entry state if there is no activity on the interconnect *based on receipt of the electrical idle ordered set;*
and...”

Emphasis added.

Yu does not expressly or inherently describe the above emphasized elements of claim 1. Yu describes a power management indication mechanism (68) to ensure that data is not lost in transmit and receive buffers when a system is placed in a power-down mode. See Col. 4, lines 30-57. Network activity is checked before power down and power management indication mechanism (68) checks the buffers to ensure they are empty. See Col 4, lines 58-68. Applicants submit that these checks are not made based on receipt of an electrical idle order set that

indicates a transmitting device coupled to the receiving device is to enter a lower power state as emphasized for claim 1 above. Rather, the checks are based on a system CPU wanting to power down without losing data stored in buffers of its network interface. Thus, Applicants request withdrawal of the claim 1 rejection under 35 U.S.C. § 102(b) as being anticipated by Yu.

Independent claims 7 and 12 also include similar elements to those emphasized above in claim 1. Additionally, claims 2-6, 8-11 and 13-16 depend from one of independent claims 1, 7, and 12. Thus, Applicants also request withdrawal of the claim 2-6, 8-11 and 13-16 rejections under 35 U.S.C. § 102(b) as being anticipated by Yu.

Conclusion

Applicant respectfully submits that claims 1-16 are in condition for allowance and such action is earnestly solicited. *The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.*

Please charge any shortages and credit any overcharges to our Deposit Account number 50-0221.

Respectfully submitted,
Puffer, et al.

Date: July 31, 2006

by: /s/Ted A. Crawford/Reg. No. 50,610/
Ted A. Crawford, Reg. No. 50,610
Patent Attorney for Assignee Intel Corporation

Intel Corporation
PO Box 5326
SC4-202
Santa Clara, CA 95056-5326
Tel. (503) 712.2799